24. (Amended) A method of removing a hard mask comprising:

forming an oxide region over or within a semiconductor substrate;

forming a silicon layer over the semiconductor substrate, wherein the silicon layer covers the oxide region;

forming and patterning a hard mask layer over the silicon layer;

etching a gap in the silicon layer to expose a portion of the oxide region using the patterned hard mask as an etch mask;

forming a sacrificial layer having a relatively planar top surface over the semiconductor substrate, the sacrificial layer comprising a portion covering the hard mask layer and a portion filling the gap; and

removing the sacrificial layer and the hard mask layer with a single etch process, wherein an etch rate of the sacrificial layer and an etch rate of the hard mask layer are selected to substantially completely remove the portion of the sacrificial layer covering the hard mask and the hard mask layer, and wherein the etch rate of the hard mask layer is substantially greater than the silicon layer.

REMARKS

Claims 1-26 are pending in the application. Claims 1 and 24 are amended with this response. Support for the amendment to claim 1 may be found in applicants' specification, for example, on pages 5-7. Reconsideration of the application in light of the following remarks is respectfully requested.

I. REJECTION OF CLAIM 24 UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

Claim 24 was rejected under 35 U.S.C. § 112, second paragraph for having insufficient antecedent basis for the term "polysilicon layer." Claim 24 has been amended to overcome the above rejection, without narrowing the scope thereof. Accordingly, withdrawal of the rejection is respectfully requested.